UTILITY PATENT APPLICATION TRANSMITTAL

☐ DUPLICATE

Address to:	Attorney Docket No.	EM/CHEN/5412
Assistant Commissioner for Patents Box PATENT APPLICATION Washington, DC 20231	First Named Inventor (or identifier)	Sun Chung CHEN
	Total Pages	61

Transmitted herewith is a patent application under 37 CFR 1.53(b).

Entitled: AN ELECTRONIC SWITCHING DEVICE FOR A UNIVERSAL SERIAL BUS INTERFACE

☒ 1. **Submitted herewith are the following:**

15 pages of specification, including Abstract.
10 sheets of formal drawings.
14 claims.
1 Oath/Declaration signed by each inventor.
1 signed Small Business Small Entity Statement.
1 Assignment of the invention, Cover Sheet, and payment of the $40.00 recordal fee.
1 certified copy of application no. 88208630 filed in Taiwan, R.O.C. Priority is claimed.
1 check in the amount of $385.00 including any assignment recordal fee.

☒ 2. **The Commissioner is authorized to credit any overpayment and charge any deficiency in any fees required under 37 CFR 1.16 and/or 1.17, to Deposit Account No. 02-0200.**

☐ 3. Insert before the first sentence of the specification: - - This application claims the benefit of provisional application number _____ filed _____. - -

☐ 4. Insert before the first sentence of the specification: - - This application is a Continuation-in-part of nonprovisional application number _____ filed _____. - -

☐ 5. Other:_____.

THE FILING FEE IS CALCULATED AS FOLLOWS:				Basic Fee:	$690.00
Total Claims:	14	- 20 =	0	X $18 =	0.00
Independent Claims:	1	- 3 =	0	X $78 =	0.00
Correspondence Address: BACON & THOMAS, PLLC 625 Slaters Lane, 4th Floor Alexandria, VA 22314-1176				Multiple Dependent Claim (add $260.00):	0.00
				Subtotal:	690.00
				50% Reduction if Small Entity Status:	345.00
Phone: 703-683-0500 Fax: 703-683-1080				Total:	345.00

Date:	Name:	Signature:	Reg. No.
February 28, 2000	Eugene Mar		25,893

S:\Producer\em\BTFORMS\utility application form.wpd (29Dec1999)

Small Business

VERIFIED STATEMENT (DECLARATION) BY A SMALL BUSINESS CLAIMING SMALL ENTITY STATUS UNDER *37 CFR 1.9(F) AND 1.27(c)*

Applicant or Patentee: Sun Chung CHEN
Docket #:
Serial or Patent Number:
Group Art Unit:
Filed or Issued:
Examiner:
Title: AN ELECTRONIC SWITCHING DEVICE FOR A UNIVERSAL SERIAL BUS INTERFACE

I hereby declare that I am

☒ the owner of the small business concern identified below:

☐ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Concern: ATEN INternational Co., Ltd.
Address: 12F, No. 101, SungChiang Rd., Taipei, Taiwan, R.O.C.

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in *13 CFR 121.3-18*, and reproduced in *37 CFR 1.9(d)*, for purposes of paying reduced fees under *section 41(a) and (b) of Title 35, United States Code*, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the matter described in:

☒ The specification filed herewith, with the title as listed above.

☐ The patent application identified above.

☐ The PCT International patent application identified above.

☐ The patent number identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under *37 CFR 1.9(c)* if that person made the invention, or by any concern who would not qualify as a small business concern under *37 CFR 1.9(d)*, or a nonprofit organization under *37 CFR 1.9(e)*. Each person or organization having any rights in the invention is listed below:

☒ no such person, concern or organization.

☐ each such person, concern or organization listed below:

FULL NAME:	☐ Individual ☐ Small Business Concern ☐ NonProfit Organization
ADDRESS:	

FULL NAME:	☐ Individual ☐ Small Business Concern ☐ NonProfit Organization
ADDRESS:	

☐ See attached sheet for additional person(s) concern(s) or organization(s).

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate *(37 CFR 1.28(b))*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under *section 1001 of Title 18 of the United States Code*, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which the verified statement is directed.

Name and Title Ching Tang CHEN	Date January 20, 2000
Address 12F, No. 101, Sung Chiang Rd., Taipei, Taiwan, R.O.C.	Signature C. T. Chen

B&T-SMLBUS.SED

AN ELECTRONIC SWITCHING DEVICE FOR A UNIVERSAL SERIAL BUS INTERFACE

FIELD OF THE INVENTION

The present invention relates to a switching device for a universal serial bus interface, and more particularly to an electronic switching device that can connect a plurality of device each having a universal serial bus interface, so as to share related resources.

BACKGROUND OF THE INVENTION

All of the conventional switching devices for a universal serial bus (USB) interface are mechanical switching devices. The switching action of the mechanical switching device is a kind of sequential switching, therefore, when the switch passes the intermediate unrelated connection points, the related electronic signal will cause unrelated devices to operate, even though the connection time is very short. When the switching between related devices is very fast, the related devices may not operate accurately.

Furthermore, a mechanical switching device is apt to form the disconnection problem, and sometimes is not very easy to twist/turn.

OBJECTS OF THE INVENTION

It is therefore an object of the present invention to provide an electronic switching device for a universal serial bus interface, such that when enabling the switch sequentially to select a related device, due to a delay signal generator design the intermediate devices will not operate.

It is another object of the present invention to provide an electronic switching device for a universal serial bus interface, so as to replace the conventional mechanical switching device to avoid the disconnection problem, and the twist/turn problem.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be better understood with the following drawings, in which:

Fig. 1 is a schematic block diagram according to a first embodiment of the present invention.

Figs. 2 is the circuit diagram of the first embodiment of the present invention.

Fig. 3 is the circuit diagram of a second embodiment according to the present invention.

Fig. 4 is the circuit diagram of a third embodiment according to the present invention.

Fig. 5 is a schematic block diagram of the first embodiment of the present invention showing that a delay signal generator is added.

Fig. 6 is a schematic circuit diagram of the first embodiment of the present invention showing that a delay signal generator is added.

Fig. 7 is a schematic block diagram of the first embodiment of the present invention showing that a display is added.

Fig. 8 is a schematic circuit diagram of the first embodiment of the present invention showing that a display is added.

Fig. 9 is a schematic block diagram of the first embodiment of the present invention showing that an enable signal generator is added.

Fig. 10 is a schematic circuit diagram of the first embodiment of the present invention showing that an enable signal generator is added.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 1, which is a schematic block diagram according to a first embodiment of the present invention. As shown in the figure, a trigger signal generator 11, a control signal generator 12, and a connector 13 are included, in which:

the trigger signal generator 11 having an output to be connected with an input of the control signal generator 12, and having a switch SW1 (please see Fig. 2) to output a trigger signal to control signal generator 12 when a user pushes the switch SW1 down;

the control signal generator 12 having an input to be connected with an output of the trigger signal generator 11, and having an ouput to be connected with an input of the connector 13, for receiving the trigger signal outputted from the trigger signal generator 11, and processing the trigger signal, then outputting a control signal to the connector 13;

the connector 13 having an input to be connected with a first universal serial bus (USB) interface 14 and a second universal serial bus (USB) interface 15, and having an output to be connected with a third universal serial bus (USB) interface 16. When the connector 13 receives the control signal outputted from the the control signal generator 12, the connector 13 will connect the third USB interface 16 with the first USB interface 14 or the second USB interface 15.

Next referring to Fig. 2, a detailed circuit of the first

embodiment according to the present invention will be described. A trigger signal generator 11, a control signal generator 12, and a connector 13 are included, in which:

the trigger signal generator 11 comprising a resistor R1, a capacitor C1, and a switch SW1. The resistor R1 and the capacitor C1 are serially connected between VCC and ground (GND). One end of the resistor R1 is connected with VCC, the other end of the resistor R1 is connected with one end of the capacitor C1, the other end of the capacitor C1 is connected with GND. One end of the switch SW1 is connected to GND, the other end of the switch SW1 is connected to where the resistor R1 is connected with the capacitor C1, having a voltage V1. Before the switch SW1 is enabled, the switch SW1 does not conduct, and voltage V1 will be maintained at a HIGH voltage; when the switch SW1 is enabled, it will conduct, voltage V1 will be connected to GND, so as to change the HIGH voltage to LOW voltage. When SW1 is opened again, voltage V1 will return to HIGH voltage due to the charging of the capacitor C1. Therefore, open/short actions of SW1 will cause the capacitor C1 charging/discharging, and make the voltage V1 HIGH/LOW so as to generate a pulse signal to be used as a trigger signal to control the control signal generator 12;

the control signal generator 12 comprising a first D FLIP-FLOP (or an equivalent circuit) U2. The clock signal input terminal CP of the first D FLIP-FLOP U2 is connected with the output of the trigger signal generator 11, while the reverse data output terminal QN is connected with the data input terminal D, and the output signal from the positive data output terminal Q is used as the control signal

of the connector 13. When the clock signal input terminal CP receives a pulse signal, the voltage of terminal D will be moved to terminal Q, while a reverse voltage of the original voltage of the termunal D will be formed at terminal QN, and the voltage of the terminal QN will then be sent back to terminal D. When the terminal CP receives the next pulse signal, the first D FLIP-FLOP U2 will repeat the above procedures. Therefore, when the terminal CP receives pulse signals continuously, the HIGH voltage and the LOW voltage will be outputted alternately, and used as the control signals for the connector 13;

the connector 13 comprising a first multiplexor U3 (or an equivalent circuit), the first set of signal input terminal X1 and Y1 is connected with the first USB interface 14, the second set of signal input terminal X2 and Y2 is connected with the second USB interface 15, the third set of signal input terminal X3 and Y3 is connected with the third USB interface 16, while a selecting signal input terminal SEL is connected with the output of the control signal generator 12, and the alternating signals outputted from the control signal generator 12 are used as the selecting signal of the first multiplexor U3. When a LOW voltage signal is inputted into the selecting signal input terminal SEL, the inputted signals to the first set of signal input terminal X1 and Y1 are outputted from the signal output terminal X3 and Y3. When a HIGH voltage signal is inputted into the selecting signal input terminal SEL, the inputted signals to the second set of signal input terminal X2 and Y2 are outputted from the signal output terminal X3 and Y3. In other words, the LOW voltage and the HIGH voltage of the selecting signal input terminal

SEL will make the first USB interface 14 and the second USB interface 15 to be connected with the third USB interface 16 respectively.

Referring to Fig. 3, which is the circuit diagram of a second embodiment according to the present invention. As shown in the figure, wherein the control signal generator 12 comprises two D FLIP-FLOPs (or equivalent circuits). The clock signal input terminal CP of the first D FLIP-FLOP U2 is connected with the output of the trigger signal generator 11, while the reverse data output terminal QN is connected with its data input terminal D. The clock signal input terminal CP of the second D FLIP-FLOP U4 is connected with the reverse data output terminal QN of the first D FLIP-FLOP U2, while the reverse data output terminal QN of the second D FLIP-FLOP U4 is connected with its data input terminal D, and the positive data output terminals Q of the first D FLIP-FLOP U2 and the second D FLIP-FLOP U4 are used as the control signals for the connector 13. When the clock signal input terminal CP of the first D FLIP-FLOP U2 receives a pulse signal, the voltage of its data input terminal D will be moved the positive data output terminal Q, while a reverse voltage of the original data input terminal D will be formed at the reverse data output terminal QN, and the voltage of the reverse data output terminal QN will then be sent back to the data input terminal D. When the next pulse signal is inputted to the control signal generator 12, the voltage of the data input terminal D will be moved to the positive data output terminal Q of the first D FLIP-FLOP U2, and now the voltage of the positive data output terminal Q is opposite to the voltage generated by the previous pulse signal inputted to the

control signal generator 12. Thus a HIGH voltage and a LOW voltage will be generated alternately. The voltage of the reverse data output terminal QN of the first D FLIP-FLOP U2 is used as a trigger signal to be inputted to the clock signal output terminal CP of the second D FLIP-FLOP U4, thus the positive data output terminal Q of the second D FLIP-FLOP U4 also generates HIGH and LOW voltages alternately, having a frequency just a half of the first D FLIP-FLOP U2's. Therefore, four patterns of LOW and LOW voltages, HIGH and LOW voltages, LOW and HIGH voltages, HIGH and HIGH voltages are obtained at the positive data output terminals Q of the first D FLIP-FLOP U2 and the second D FLIP-FLOP U4, and are outputted alternately as the control signals to let the connector 13 connect different USB interfaces.

Referring to Fig. 4, which is the circuit diagram of a third embodiment according to the present invention. The difference between the circuit in Fig. 4 and the aforementioned electronic switching device for USB interface is the internal resistance in the connector 13. As shown in the figure, a first multiplexor U3 and a second multuplexor U3'are parallelly connected in the connector 13, so as to decerase the internal resistance in connector 13, therefore, the quality of the signal transmmision between USB interfaces are enhanced, and the distance between USB interfaces can be increased.

Referring to Figs. 5 and 6, which are the schematic block diagram and the circuit diagram of the first embodiment of the present invention showing that a delay signal generator 17 is added. As shown in the figures, the delay signal generator 17 comprises a resistor R2, a capacitor C2 and a diode D1 (see Fig. 6), having its

input to be connected with the output of the trigger signal generator 11, and its output to be connected with the enable terminal OE of the connector 13. The resistor R2 and the capacitor C2 are serially connected between VCC and GND, one end of the resistor R2 is connected with VCC, while the other end thereof is connected with one end of the capacitor C2, having a voltage V2, the other end of the capacitor C2 is connected to GND, the positive terminal of the diode D1 is connected with the voltage V2, while the negative terminal thereof is connected with one end of the resistor R3, the other end of the resistor R3 is the input terminal for the delay signal generator 17, and V1 (the output of the trigger signal generator 11) is used as the input of the delay signal generator 17, V2 is the output of the delay signal generator 17.

When the switch SW1 of the trigger signal generator 11 is conducting, the voltage V1 will be changed from HIGH voltage to LOW voltage, so the voltage V2 will also be changed from HIGH voltage to LOW voltage. When the switch SW1 of the trigger signal generator 11 is opened, the voltage V1 will be changed from LOW voltage to HIGH voltage, so the voltage V2 will also be changed from LOW voltage to HIGH voltage. In order to delay the time of V2 from LOW voltage to HIGH voltage, the present invention selects a capacitor having a longer time constant as the second capacitor C2. When the switch SW1 of the trigger signal generator 11 is conducting, the enable terminal OE of the connector 13 will be LOW voltage, thus the USB interfaces are all disconnected. After a while, the voltage V2 will be changed from LOW voltage to HIGH voltage, and the related USB interfaces are connected according to the control

signals outputted from the control signal generator 12. The design of the present invention is to let the user turn the switch sequentially to select the required USB interface connection (e.g. push the switch button once to select the first device, and push the switch button twice to select the second device). However, if a user pushes the switch several times quickly, the unrelated intermediate USB interfaces might be conducting to cause signal confusing and disable the whole system, therefore, a delay signal generator 17 is needed to avoid unrelated device to react due to the delay saturation of the voltage V2.

Referring to Figs. 7 and 8, which are the schematic circuit block diagram and the circuit diagram of the first embodiment of the present invention showing that a display 18 is added. As shown in the figures, the input of the display 18 is connected with the output of the control signal generator 12, the different signals outputted from the control signal generator 12 will make LED 1, LED 2 conducting respectively, so as to show the connections between different USB interfaces.

Referring to Figs. 9 and 10, which are the schematic circuit block diagram and the circuit diagram of the first embodiment of the present invention showing that an enable signal generator 19 is added. As shown in the figure, the output of the enable signal generator 19 is connected with the control signal generator 12. The enable signal generator comprises a resistor R4 and a capacitor C4, wherein the resistor R4 and the capacitor C4 are serially connected between VCC and GND. One end of the resistor R4 is connected to GND, while the other end thereof is connected with one end of the capacitor C4,

having a voltage V3. The other end of the capacitor C4 is connected with VCC. When VCC is conducting, V3 will be changed from LOW voltage to HIGH voltage immediately, and sent to the reset terminal R of the first D FLIP FLOP U2 of the control signal generator 12 to clear the output of the first D FLIP FLOP U2 to LOW voltage. After a while, since the capacitor C4 is charged, V3 will be changed from HIGH voltage to LOW voltage, and maintained at LOW voltage, and the control signal generator 12 will not be influenced by the enable signal generator 19. Thus the connections between different USB interfaces are the same whenever the VCC begins conducting.

Furthermore, VCC will be used as the HIGH voltage of the present invention, no other power supply is needed, and a diode can be connected between VCC and each USB interface to avoid the reverse current flowing from USB interface to VCC.

In addition, the pulse signal outputted from the trigger signal generator 11 can be a positive or a negative pulse signal, and the number of the control signal outputted from the control signal generator is not limited. The numbers of the display, multuplexors and USB interfaces are also not limited.

The above embodiments are only used for description, and can not be treated as a limitation. The spirit and scope of the present invention will only be limited by the appended claims.

WHAT IS CLAIMED IS:

1. An electronic switching device for a universal serial bus (USB) interface, comprising a trigger signal generator, a control signal generator, and a connector, wherein:

the trigger signal generator having an output to be connected with an input of the control signal generator, and having a switch to output a trigger signal to the control signal generator when a user enables the switch;

the control signal generator having an input to be connected with an output of the trigger signal generator, and having an ouput to be connected with an input of the connector, for receiving the trigger signal outputted from the trigger signal generator, and processing the trigger signal, then outputting a control signal to the connector;

the connector having an input to be connected with each universal serial bus (USB) interface of at least two electronic devices, and having an output to be connected with a universal serial bus (USB) interface of another electronic device, when the connector receives the control signal outputted from the the control signal generator, the connector will connect related universal serial bus (USB) interfaces according to the control signal.

2. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the trigger signal generator comprising a resistor, a capacitor, and a switch, the resistor and the capacitor are serially connected between a power supply and a ground, one end of the switch is connected to the ground, the other end of the switch is connected to where the resistor and the capacitor are connected, enabling the switch to generate a pulse signal to be

used as the trigger signal.

3. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the control signal generator comprising a D FLIP-FLOP, having a clock signal input terminal to be used as the input of the control signal generator, and having a reverse data output terminal to be connected with a data input terminal thereof, a positive data output terminal thereof is used as the output of the control signal generator.

4. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the connector comprising a multiplexor, an input and an output of the multiplexor are connected respectively with each universal serial bus (USB) interface of different electronic devices, and a selecting signal input terminal thereof is connected with the output of the control signal generator.

5. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the control signal generator comprising at least two D FLIP-FLOPs, a clock signal input terminal of the first D FLIP-FLOP is connected with the output of the trigger signal generator, while a reverse data output terminal is connected with its data input terminal; a clock signal input terminal of the second D FLIP-FLOP is connected with the reverse data output terminal of the first D FLIP-FLOP, while a reverse data output terminal of the second D FLIP-FLOP is connected with its data input terminal; and so on; and the positive data output terminals of all the D FLIP-FLOPs are used as the control signals for the connector.

6. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the connector comprising at

least two identical multiplexors to be parallely connected for decreasing the internal resistance in the connector.

7. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein a delay signal generator is provided between the trigger signal generator and the connector, having an input to be connected with the output of the trigger signal generator, and having an output to be connected with tan enable terminal of the connector.

8. An electronic switching device for a universal serial bus (USB) interface according to claim 7, wherein the delay signal generator comprising two resistors, a capacitor and a diode, having its input to be connected with the output of the trigger signal generator, and having its output to be connected with the enable terminal of the connector, the first resistor and the capacitor are serially connected between a power supply and a ground, a point where the first resistor and the capacitor are connected is connected with a positive terminal of the diode and the enable terminal of the connector, while a negative terminal of the diode is connected with one end of the second resistor, the other end of the second resistor is the input terminal of the delay signal generator.

9. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the control signal generator is connected with a display for showing the current connections of the universal serial bus (USB) interfaces.

10. An electronic switching device for a universal serial bus (USB) interface according to claim 9, wherein the display comprising light emitting diodes.

11. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the control signal generator is connected with an enable signal generator so that the connections between different USB interfaces are the same whenever the power supply begins conducting.

12. An electronic switching device for a universal serial bus (USB) interface according to claim 11, wherein the enable signal generator comprising a resistor and a capacitor, the resistor and the capacitor are serially connected between the power supply and the ground, a point where the resistor and the capacitor are connected is used as an output to be connected with a reset terminal of the control signal generator.

13. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein the power supply used by the electronic switching device for a universal serial bus (USB) interface is the power supply used by the connected universal serial bus (USB) interface.

14. An electronic switching device for a universal serial bus (USB) interface according to claim 1, wherein a diode is connected between the power supply and each USB interface to avoid the reverse current flowing from USB interface to the power supply.

ABSTRACT OF THE DISCLOSURE

The present invention provides an electronic switching device for a universal serial bus (USB) interface, which can connect several different electronic devices each having a universal serial bus (USB) interface when needed. By manually enabling a switch of the electronic switching device for a universal serial bus (USB) interface, a trigger signal generated from a trigger signal generator will be outputted to a control signal generator to generate a control signal for connecting related electronic devices. A delay signal generator can be added to avoid the intermediate devices being operated unintentionally.

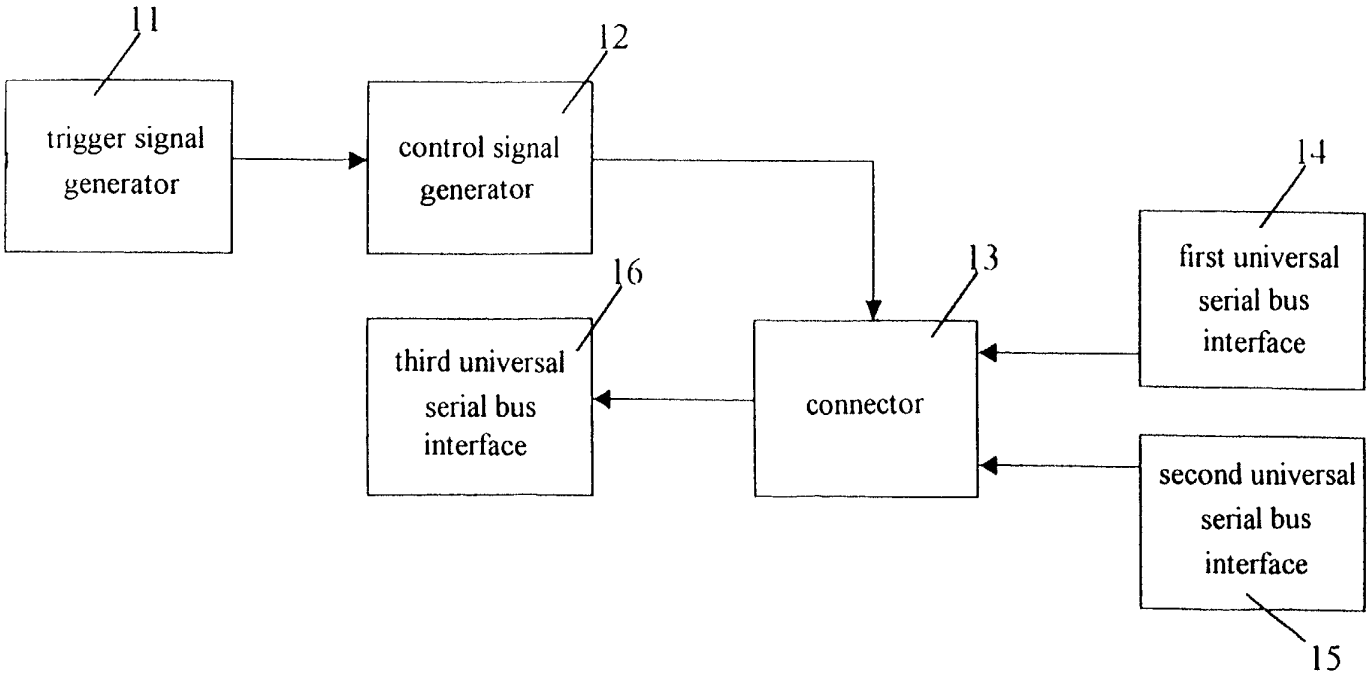
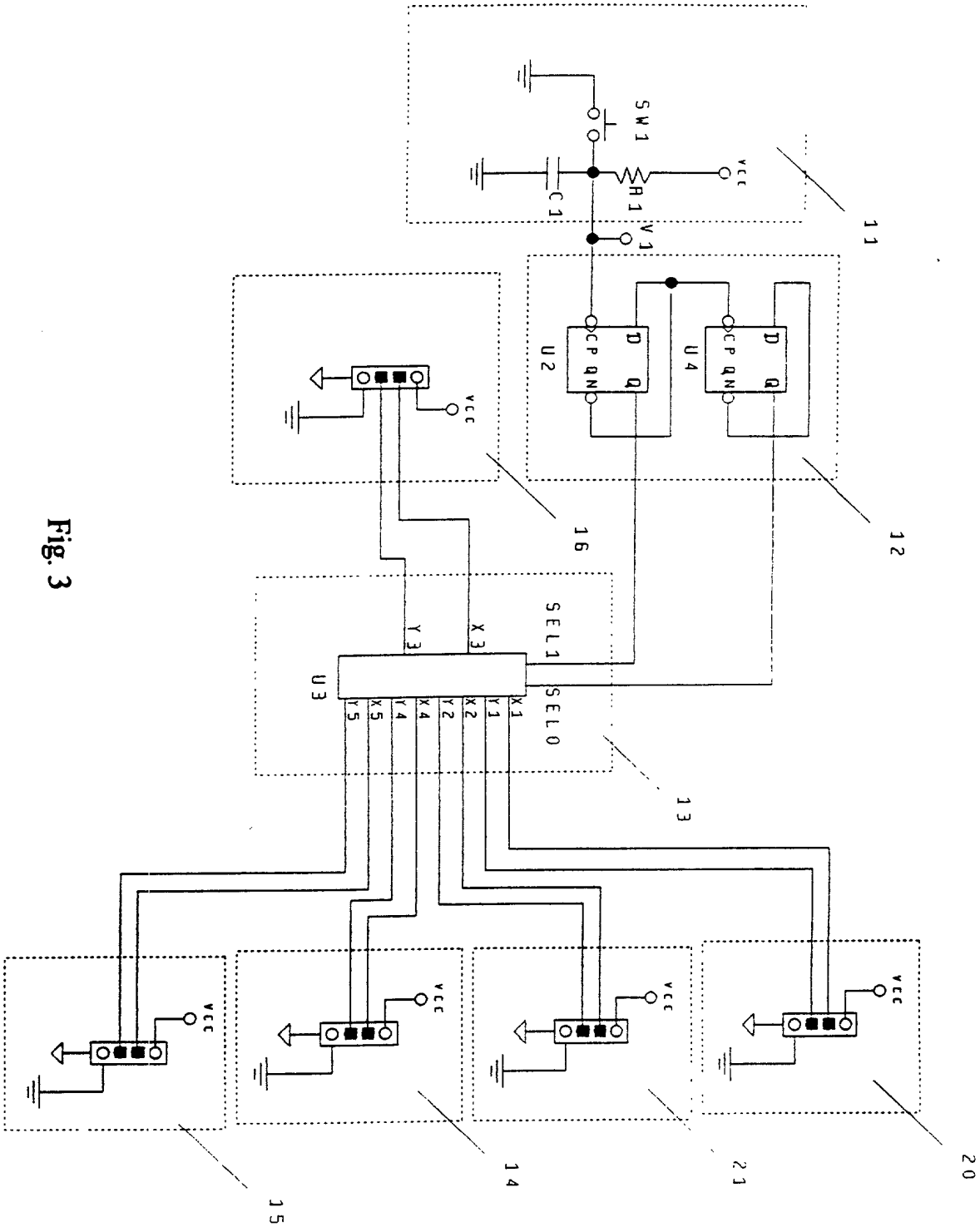

11
trigger signal generator
12
control signal generator
14
first universal serial bus interface
16
third universal serial bus interface
13
connector
second universal serial bus interface
15

Fig. 1

Fig. 2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C1
R1
V1
VCC
11
U2
U4
D
CP
QN
Q
12
16
SEL1
SEL0
U3
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Y4
Y5
13
14
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20
21

Fig. 3

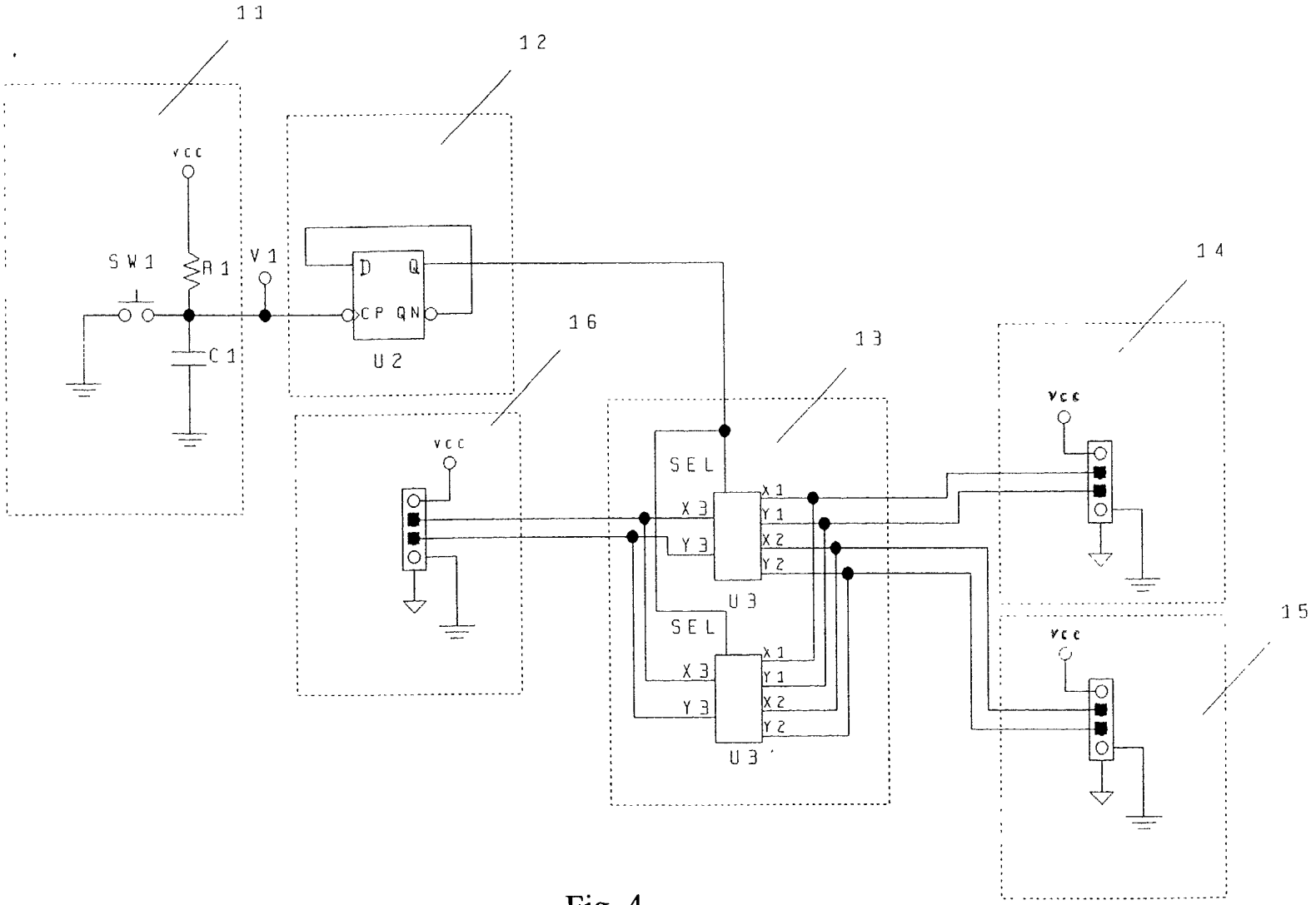


Fig. 4

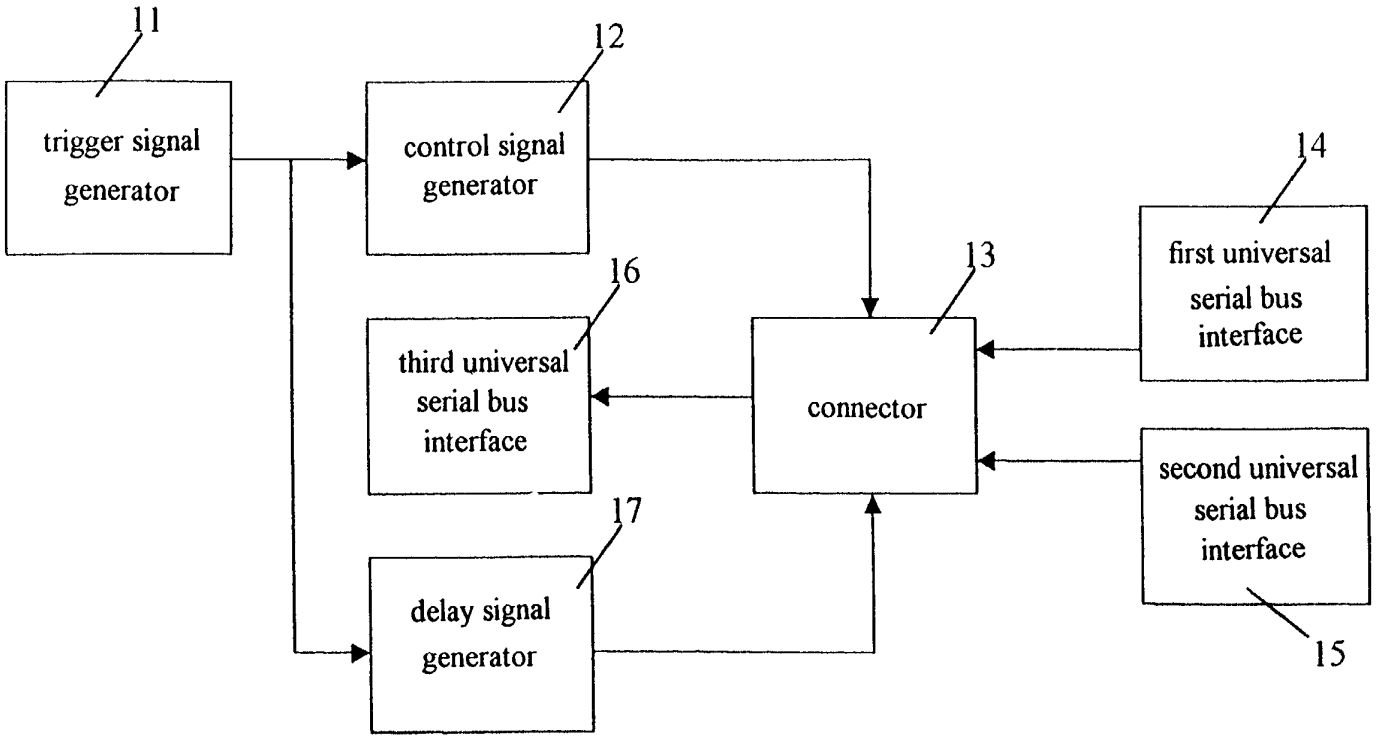

11
trigger signal generator
12
control signal generator
14
first universal serial bus interface
13
connector
16
third universal serial bus interface
second universal serial bus interface
17
delay signal generator
15

Fig. 5

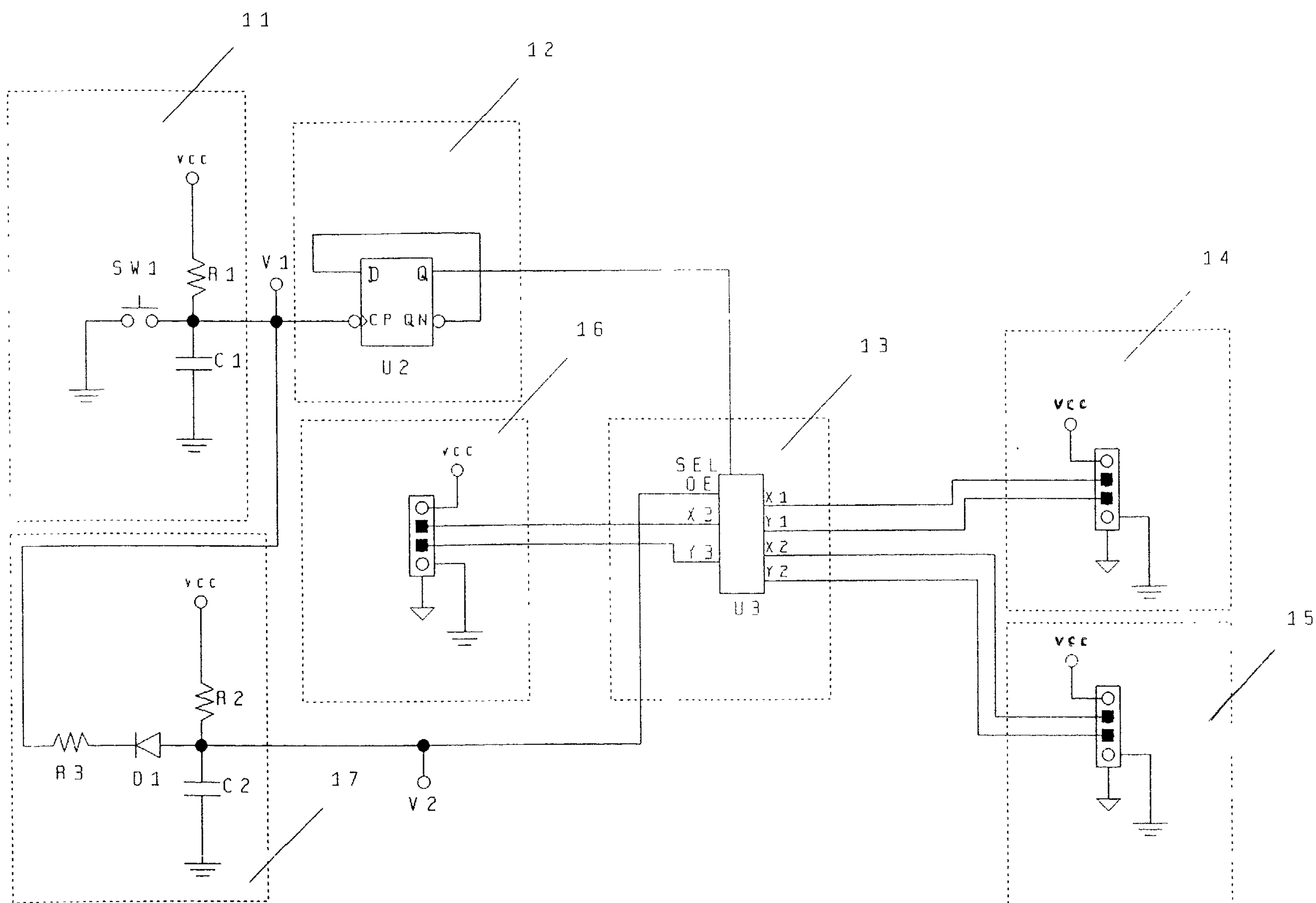


Fig. 6

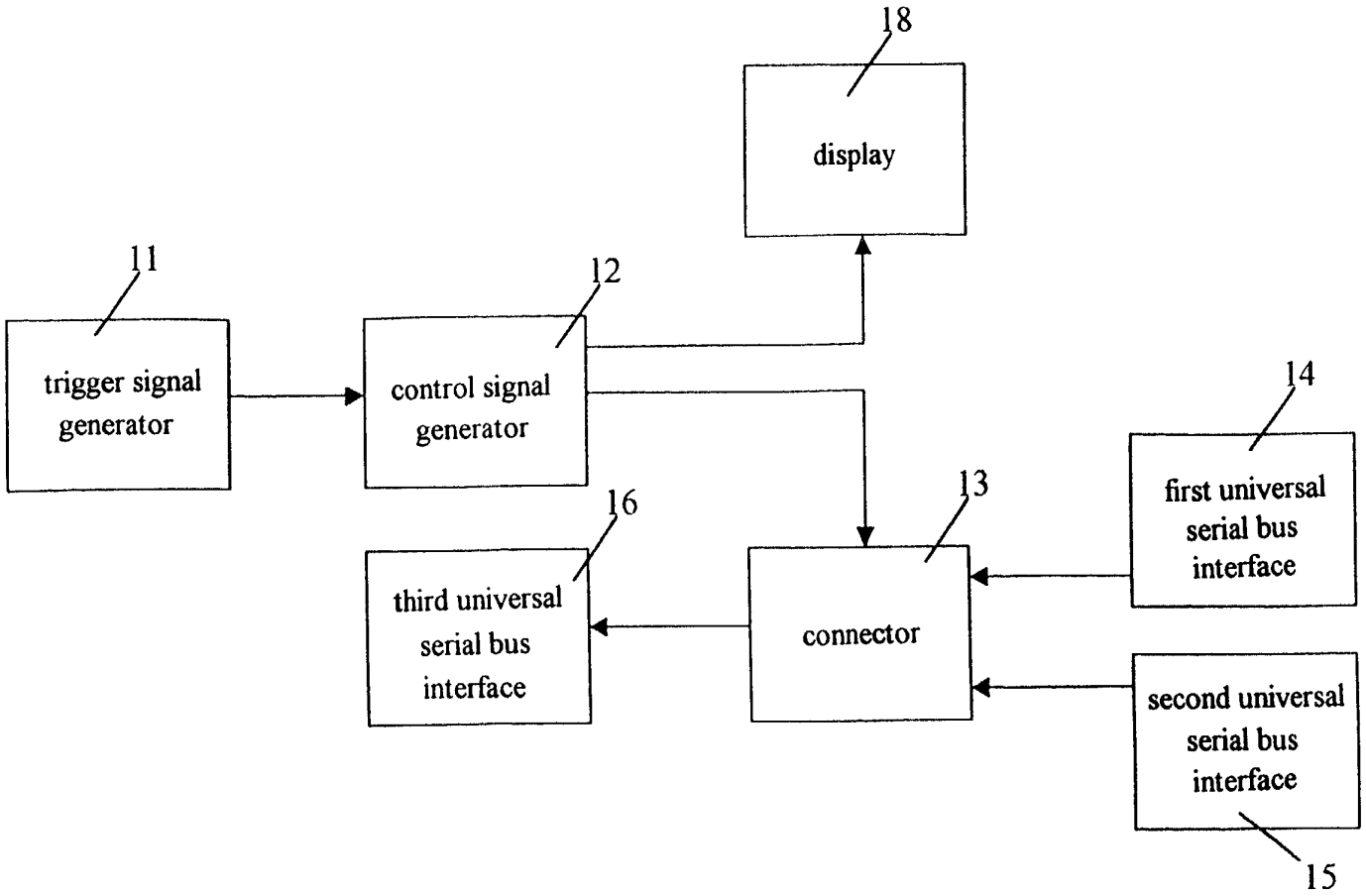
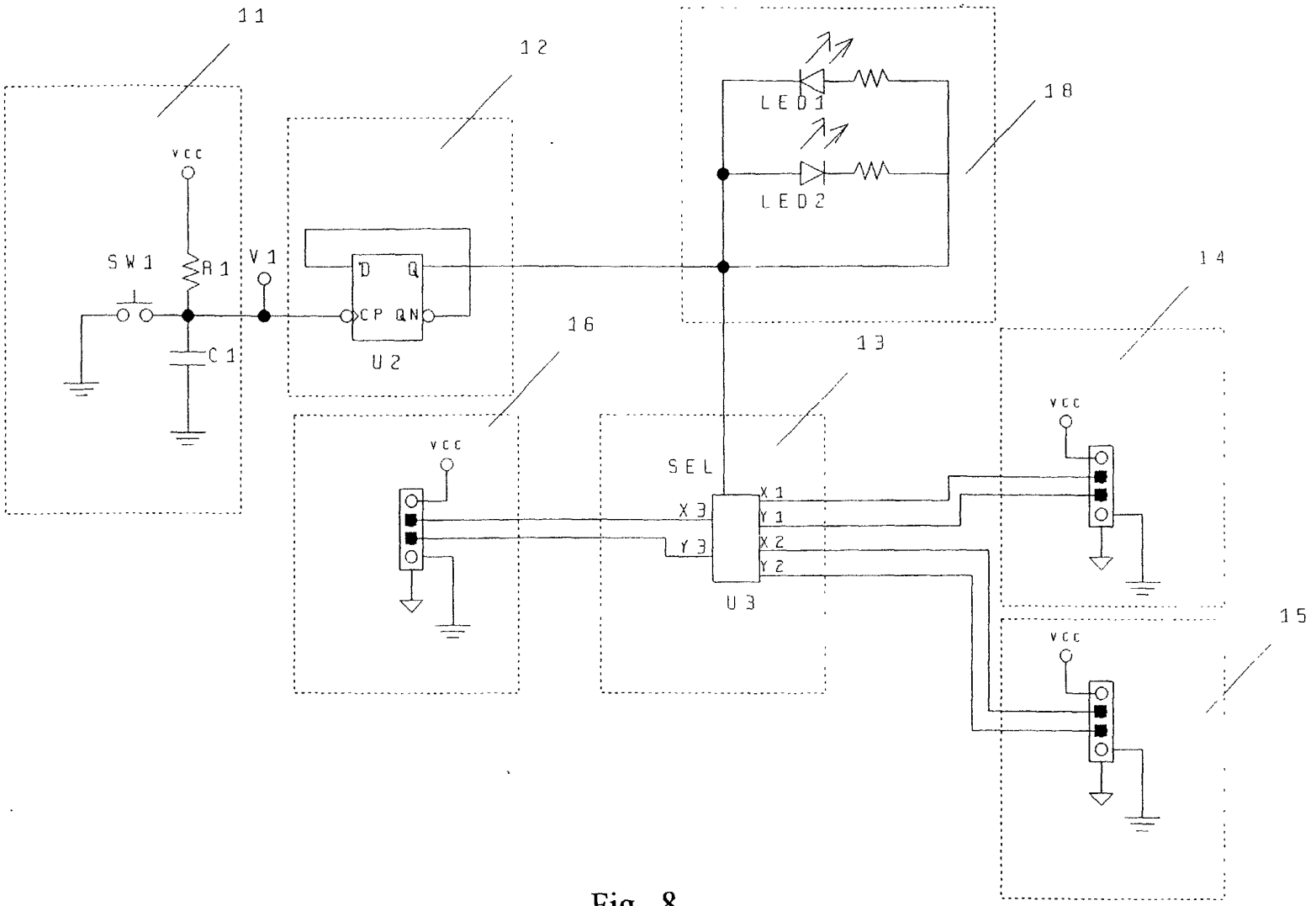

18
display
11
12
trigger signal generator
control signal generator
14
first universal serial bus interface
13
16
third universal serial bus interface
connector
second universal serial bus interface
15

Fig. 7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12
18
14
16
13
15
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SW1
R1
V1
C1
D
Q
CP
QN
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Y3
X1
Y1
X2
Y2
U3

Fig. 8

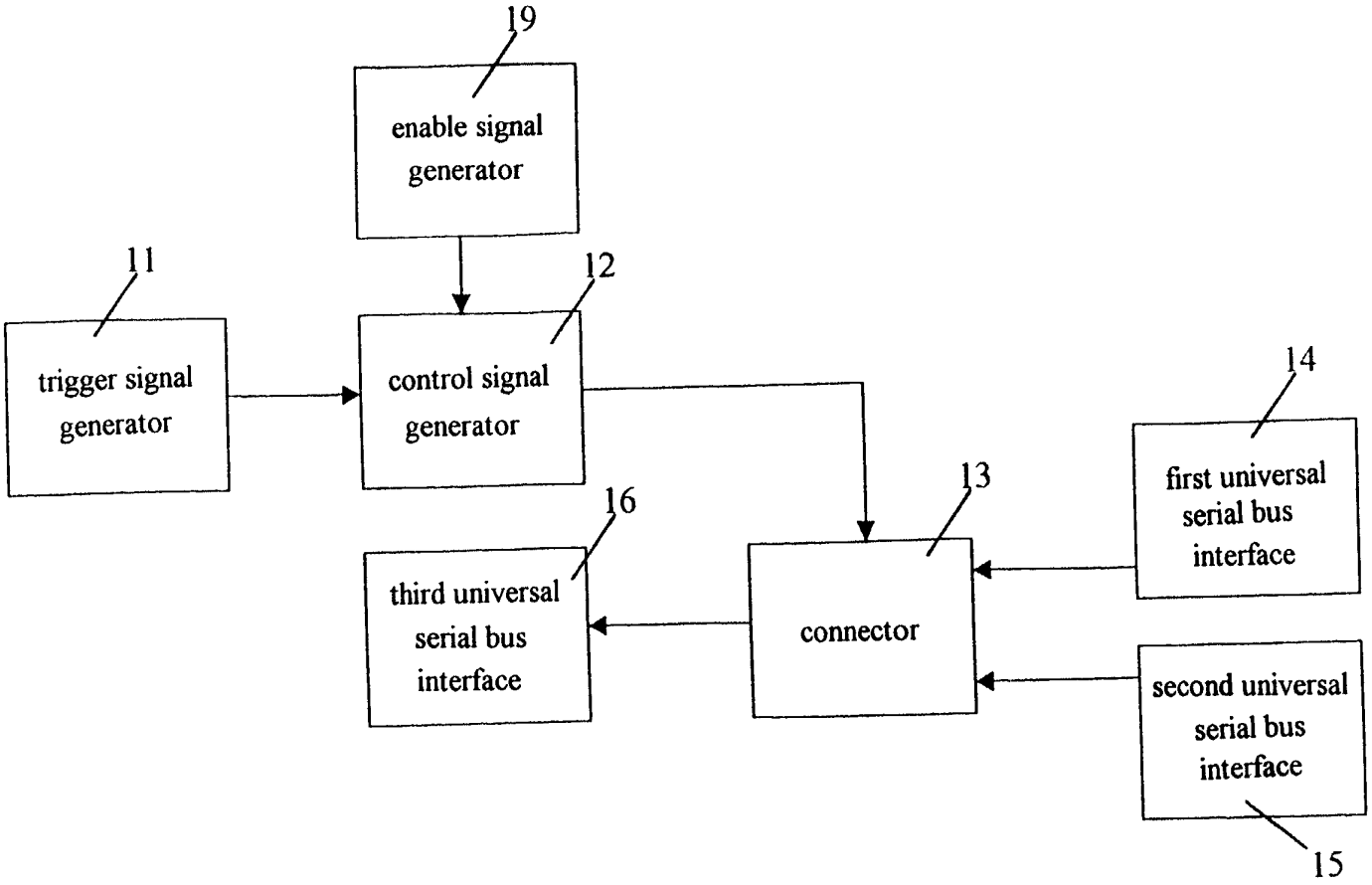
19
enable signal generator
11
trigger signal generator
12
control signal generator
14
first universal serial bus interface
13
16
third universal serial bus interface
connector
second universal serial bus interface
15

Fig. 9

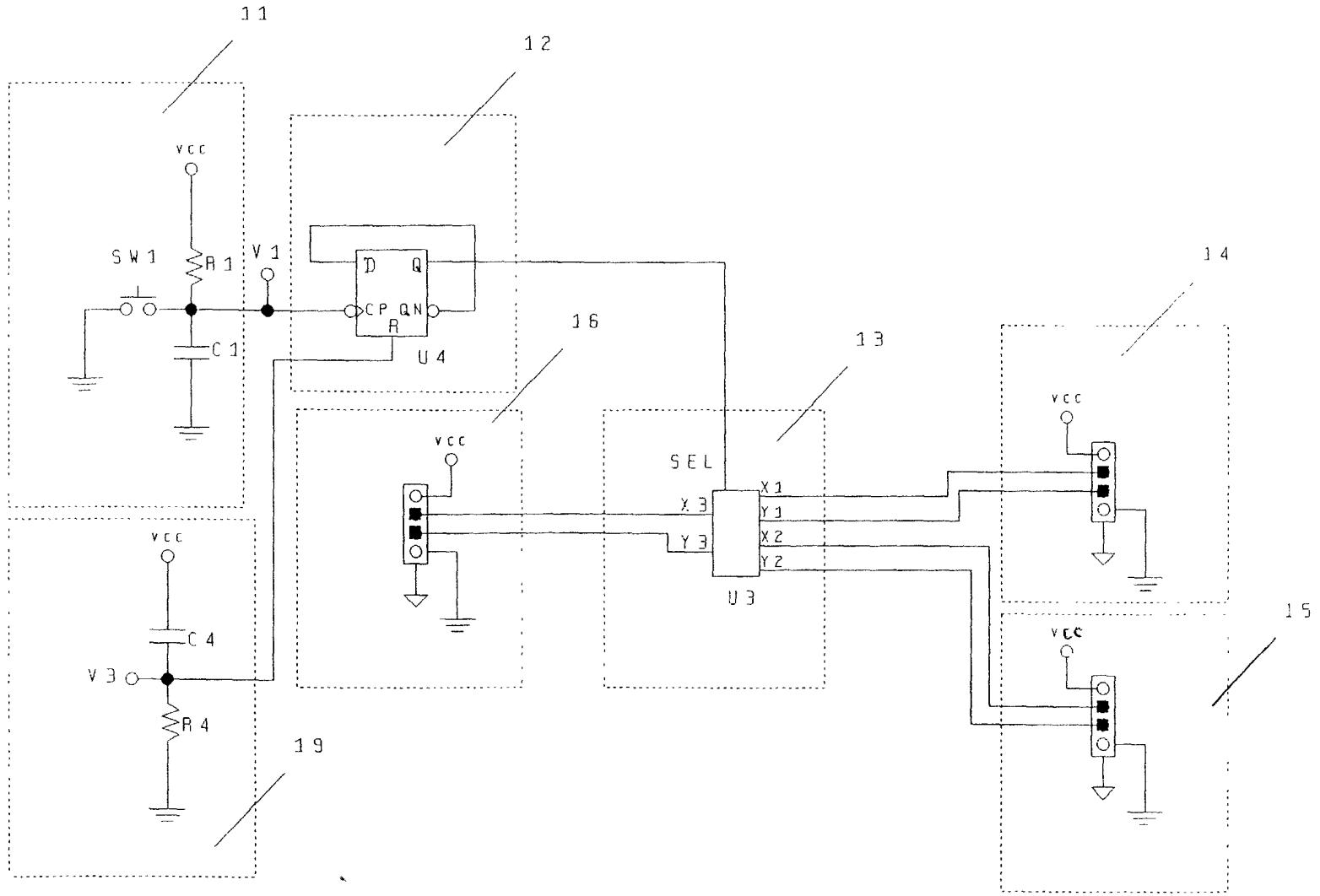

Fig. 10

ATTORNEY/DOCKET NO:

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

AN ELECTRONIC SWITCHING DEVICE FOR A UNIVERSAL SERIAL BUS INTERFACE

the specification of which (check one):

☒ is attached hereto, or ☐ was filed on: as U.S. Application Number or PCT International Application Number:

and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56*. I hereby claim foreign priority benefits under *Title 35, United States Code §119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No
88208630	TAIWAN, R.O.C.	May 28, 1999	X	

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE §119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	Day/Month/Year Filed

☐ Additional Provisional Application(s) Listed on Following Page(s)

☐ I hereby claim the benefit under *Title 35, United States Code, §120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code, §112*, I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

☐ Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Charles R. Wolfe, Jr., Reg. No. 28,680; Thomas J. Moore, Reg. No. 28,974; Joseph DeBenedictis, Reg. No. 28,502; Benjamin E. Urcia, Reg. No. 33,805; Chung C. Chen, Reg. No. 31,725; and

I(we) authorize my(our) attorneys to accept and follow instructions from U.S. PATENT & TRADEMARK OFFICE regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I(we) or my(our) assigns withdraw this authorization in writing.

Send correspondence to: **BACON & THOMAS, PLLC**
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FULL NAME OF FIRST OR SOLE INVENTOR	CITIZENSHIP
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DATE January 20, 2000	SIGNATURE

☐ *See following page(s) for additional joint inventors.*